

CLAIMS

WHAT IS CLAIMED IS:

1. A logic circuit for use in a multiplexor to shift data, comprising:
a plurality of logic gates, each logic gate receiving data inputs and control signals;
and
a plurality of shared data lines connecting the logic gates, the shared data lines providing a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates,
wherein the logic gates shift data received at the data inputs based upon the control signals and the connections of the shared data lines to produce a shifted data output.
2. The logic circuit of claim 1 wherein each of the logic gates includes first and second stages of shifting performing first and second shift operations.
3. The logic circuit of claim 2 wherein each of the logic gates includes control inputs for receiving two sets of shift control signals for the first and second stages of shifting.
4. The logic circuit of claim 3, further including another plurality of shared data lines for providing data inputs to the second stage of shifting for the second shift operation.

5. The logic circuit of claim 1 wherein the plurality of shared data lines connect adjacent logic gates among the plurality of logic gates.
6. The logic circuit of claim 1 wherein each of the logic gates receives as one of the data inputs a primary data line.
7. The logic circuit of claim 1 wherein each of the logic gates receives a clocking signal for enabling the logic gates to feed data.
8. The logic circuit of claim 1 wherein each of the logic gates includes a plurality of transistors, controlled by the control signals, for feeding data from the shared data lines into the logic gate.
9. The logic circuit of claim 1 wherein each of the logic gates provides complementary outputs as the shifted data output.
10. The logic circuit of claim 1 wherein each of the shared data lines connects one of the logic gates with a plurality of the logic gates.
11. ~~A method of using a multiplexor to shift data, comprising:~~
providing a plurality of logic gates each receiving data inputs and control signals;

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connecting the logic gates using a plurality of shared data lines providing a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates; and

shifting data received at the data inputs based upon the control signals and the connections of the shared data lines to produce a shifted data output.

12. The method of claim 11 wherein the shifting step includes shifting the data through first and second stages of shifting performing first and second shift operations.

13. The method of claim 12 wherein the providing step includes receiving two sets of shift control signals for the first and second stages of shifting.

14. The method of claim 13, further including connecting the logic gates using another plurality of shared data lines for providing data inputs to the second stage of shifting for the second shift operation.

15. The method of claim 11 wherein the connecting step includes connecting adjacent logic gates among the plurality of logic gates.

16. The method of claim 11 wherein the providing step includes receiving as one of the data inputs a primary data line.

17. The method of claim 11 wherein the providing step includes receiving a clocking signal for enabling the logic gates to feed data.

18. The method of claim 11 wherein the shifting step includes feeding data from the shared data lines into the logic gates using transistors controlled by the control signals.

19. The method of claim 11 wherein the shifting step includes providing complementary outputs as the shifted data output.

20. The method of claim 11 wherein the connecting step includes connecting one of the logic gates with a plurality of the logic gates.